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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/758,863	01/16/2004	Robert B. Staszewski	TI-35773	6568

23494 7590 09/24/2007
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EXAMINER	
FLORES, LEON	

ART UNIT	PAPER NUMBER
2611	

NOTIFICATION DATE	DELIVERY MODE
09/24/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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ND

Office Action Summary	Application No.	Applicant(s)
	10/758,863	STASZEWSKI ET AL.
	Examiner	**Art Unit**
	Leon Flores	2611

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _20 July 2007_.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-47_ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-47_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _16 January 2004_ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims (1-47) have been considered but are moot in view of the new ground(s) of rejection.

Response to Remarks

Applicant asserts that, *"Claim 32 requires, "circuitry to manipulate digital signals from the RF circuit to provide a performance metric for the RF circuit .... " Wong teaches only circuit testing and does not teach that a metric is generated representing the estimated performance of the RF circuit".*

The examiner respectfully disagrees. One skilled in the art would know that the performance of the device can be analyzed and viewed using this type of testing device.

Applicant asserts that, *"Claim 41 requires, "the phase detector containing circuitry to compute a difference between the reference phase and a variable phase .... " Wong only teaches UP/DOWN phase direction information, which is not the phase error estimation signal".*

The examiner respectfully disagrees. One skilled in the art would know that unit 10, in figure 2, is capable of computing the phase error between the incoming signal and the feedback signal. However, taking the contrary, the examiner has issued a new ground of rejection in order to substantiate for this limitation.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims (32-34, 37-40) are rejected under 35 U.S.C. 102(b) as being anticipated by Wong et al. (hereinafter Wong) (US Patent 5,295,079)

Re claim 32, Wong discloses a circuit comprising: a processor coupled to a radio frequency (RF) circuit, the processor containing circuitry to manipulate digital signals from the RF circuit to provide a performance metric for the RF circuit (See fig. 2: 4 & col. 1, lines 45-48, 56-61, col. 2, lines 36-40, col. 4, lines 6-15); and a control signal input coupled to the processor, wherein the control signal input can enable an observation and manipulation of the digital signals. (See fig. 1: the input of element 4 & col. 1, lines 56-61)

Re claim 33, the combination of Wong and Girardeau further discloses a latch coupled to the processor, the latch to store the performance metric provided by the processor. (In Wong, see col. 4, lines 12-14 "microprocessor-based controller". One skilled in the art would know that latches are the most basic storage elements, from which flip-flops are usually constructed. And registers, which are used extensively in the design of digital systems for storing data, consists of a set of flip-flops.)

Re claim 34, the combination of Wong and Girardeau further discloses that wherein the RF circuit is integrated onto a first integrated circuit, wherein the processor is integrated onto a second integrated circuit. (In Wong, see fig. 2)

Re claim 37, the combination of Wong and Girardeau further discloses that wherein the RF circuit contains an all-digital phase-locked loop, and wherein the processor is coupled to a filtered output of a phase detector. (In Wong, see fig. 2: 24 & col. 3, lines 19-22, 50-56)

Re claim 38, the combination of Wong and Girardeau further discloses that wherein the RF circuit contains an all-digital phase-locked loop, and wherein the processor is coupled to an output of a phase detector and a filtered output of a phase detector. (In Wong, see col. 3, lines 50-55 & Girardeau, see fig. 1, element 18)

Re claim 39, the combination of Wong and Girardeau further discloses that wherein the circuit permits the testing of the RF circuit in wafer, in packaged integrated circuit, in factory, and in field. (In Wong, see col. 1, lines 38-41, 48-51 & col. 4, lines 16-27)

Re claim 40, the combination of Wong and Girardeau further discloses that wherein the circuit permits the testing of the RF circuit, and wherein the testing is of a type selected from a group consisting of a phase trajectory error, a frequency lock, a

frequency deviation, a phase noise power, or combinations thereof. (In Wong, see fig. 2, 4b & 4c)

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims (1, 3-8, 11, 13-17, 19-22, 24, 27-31, 41, 43, 45-46) are rejected under 35 U.S.C. 103(a) as being unpatentable over Girardeau, Jr. (hereinafter Girardeau) (US Patent 5,486,792) in view of Yamaguchi et al. (hereinafter Yamaguchi) (US Patent 6,687,629 B1)

Re claim 1, Girardeau discloses a method for testing a radio frequency (RF) circuit comprising: observing a signal from the RF circuit, wherein the signal is a digital signal from within a processing portion of the RF circuit (See fig. 2: 104), wherein the signal has a high degree of correlation with an RF output of the RF circuit (See fig. 1:

the output of 23. Furthermore, it is well known in the art that both transmitters and receivers have PLLs) and manipulating the signal (See fig. 1: 23 & 24); and producing a metric for the test based on results from the manipulating. (See fig. 1: 40 & 42 or 58 & 60)

But the reference of Girardeau fails to specifically disclose that wherein the observing occurs outside of the RF circuit.

However, Yamaguchi does. (See fig. 29) Yamaguchi discloses a spectrum analyzer connected to the output of the phase detector.

Therefore, taking the combined teachings of Girardeau and Yamaguchi as a whole. It would have been obvious to one of ordinary skills in the art to have incorporated this feature into the system of Girardeau, in the manner as claimed and as taught by Yamaguchi, for the benefit of optimizing the performance of the PLL.

Re claim 3, the combination of Girardeau and Yamaguchi further discloses that wherein the signal is a phase error signal. (In Girardeau, see fig. 1: 12, col. 2, lines 50-56)

Re claim 4, the combination of Girardeau and Yamaguchi further discloses that wherein the signal has a high degree of correlation with an RF output of the RF circuit. (One skilled in the art would know that if the input signal remains within a predetermined frequency, the PLL will produce an output signal having a frequency that is proportional

to the clock input signal's frequency. Furthermore, when the PLL is in a lock mode, the output signal and the input signal are the same.)

Re claim 5, the combination of Girardeau and Yamaguchi further discloses that wherein a transfer function between the signal and the RF output phase is flat within a frequency band of interest. (One skilled in the art would know that if the output signal has a frequency that is proportional to the clock input signal's frequency, and if their similarities or relatedness are very high, then we can say that the output is some constant multiplied by the input. Furthermore, when the PLL is in a lock mode, the output signal and the input signal are the same.)

Re claim 6, the combination of Girardeau and Yamaguchi further discloses that wherein the RF circuit is an all-digital circuit, and wherein the signal is an output of a component in an all-digital phase-locked loop in the RF circuit. (In Girardeau, see fig. 1 & col. 2, lines 54-56)

Re claim 7, the combination of Girardeau and Yamaguchi further discloses that wherein the signal is an output of a phase detector. (In Girardeau, see fig. 1 & col. 2, lines 54-56)

Re claim 8, the combination of Girardeau and Yamaguchi further discloses that wherein the signal has been filtered. (In Girardeau, see fig. 1: 24 & col. 2, lines 62-65)

Re claim 11, the combination of Girardeau and Yamaguchi further discloses that wherein a loop filter coupled to an output of a phase detector performs the filtering, and wherein the signal is an output of the loop filter. (In Girardeau, see fig. 1: 24 & col. 2, lines 62-65)

Re claim 13, the combination of Girardeau and Yamaguchi further discloses that wherein the frequency of the signal is several orders of magnitude less than the frequency of the RF output. (It is inherent that the frequency of the error signal, outputted from the phase comparator, is less than the RF frequency.)

Re claim 14, the combination of Girardeau and Yamaguchi further discloses that wherein the test is for phase error trajectory and the signal is the output of a phase detector (In Girardeau, see fig. 1 & col. 2, lines 54-56), and wherein the manipulation comprises measuring a change in the signal. (In Girardeau, see fig. 2: error signal. And see col. 5, lines 37-39)

Re claim 15, the combination of Girardeau and Yamaguchi further discloses that wherein if the change in the signal is less than a specified threshold, then the phase error trajectory is good. (In Girardeau, see fig. 2: error signal. And see col. 5, lines 37-

39)

Re claim 16, the combination of Girardeau and Yamaguchi further discloses that wherein the measuring the change in the signal comprises measuring a peak, a variance, or a rate of change in the signal. (In Girardeau, see fig. 2: error signal. And see col. 5, lines 37-39)

Re claim 17, the combination of Girardeau and Yamaguchi further discloses that wherein the test is for frequency lock and the signal is the output of a phase detector (In Girardeau, see col. 2, lines 30-37 & col. 4, lines 65-67), and wherein the manipulation comprises comparing a value of the signal over several samples. (In Girardeau, see fig. 2 & col. 5, lines 37-40. The error signal is being compared with the threshold.)

Re claim 19, the combination of Girardeau and Yamaguchi further discloses that wherein the samples are taken at different times. (In Girardeau, see fig. 2 & col. 5, lines 37-40. The error signal is being compared with the threshold.)

Re claim 20, the combination of Girardeau and Yamaguchi further discloses that wherein the test is for frequency deviation and the signal is an output of an integral accumulator of a loop filter (In Girardeau, see col. 5, lines 19-21), and wherein the manipulation comprises comparing the signal with a specified range. (In Girardeau, see

col. 2, lines 30-36)

Re claim 21, the combination of Girardeau and Yamaguchi further discloses that wherein if the signal is within the specified range, then the frequency deviation is within acceptable limits. (In Girardeau, see col. 2, lines 30-36)

Re claim 22, the combination of Girardeau and Yamaguchi further discloses that wherein the manipulation further comprises comparing several samples of the signal. (In Girardeau, see fig. 2 & col. 5, lines 37-40. The error signal is being compared with the threshold.)

Re claim 24, the combination of Girardeau and Yamaguchi further discloses that wherein the RF circuit contains an all-digital phase-locked loop, and the method further comprises prior to the observing, setting the all-digital phase-locked loop to a certain bandwidth. (In Girardeau, see col. 5, lines 19-21. Furthermore, it is inherent that the loop bandwidth, also referred as the unity loop gain frequency, of the phase lock loop is set prior to start up.)

Re claim 27, the combination of Girardeau and Yamaguchi further discloses that wherein the RF circuit is an all-digital frequency synthesizer. (In Girardeau, see col. 5, line 20)

Re claim 28, the combination of Girardeau and Yamaguchi further discloses that wherein the RF circuit is an all-digital transmitter. (In Girardeau, see col. 1, lines 24-27)

Re claim 29, the combination of Girardeau and Yamaguchi further discloses that wherein the transmitter is used in a wireless communications network. (In Girardeau, see col. 1, lines 24-27)

Re claim 30, the combination of Girardeau and Yamaguchi further discloses that wherein the wireless communications network is Bluetooth compliant. (In Girardeau, see col. 1, lines 24-27. It is inherent that the network is Bluetooth compliant.)

Re claim 31, the combination of Girardeau and Yamaguchi further discloses that wherein the testing comprises a functional test or a compliance test of the RF circuit. (In Girardeau, see col. 2, lines 30-37 & col. 5, lines 10-21)

Re claim 41, the motivation for combining these two references has already been established in claim 1 above, therefore, the combination of Girardeau and Yamaguchi further discloses a circuit comprising: a reference phase accumulator coupled to a signal input, the reference phase accumulator containing circuitry to compute a reference phase (In Girardeau, see fig. 1: 26); a phase detector coupled to the reference phase accumulator, the phase detector containing circuitry to compute a difference between the reference phase and a variable phase (In Girardeau, see fig. 1:

12); a digitally-controlled oscillator (DCO) coupled to the phase detector (In Girardeau, see fig. 1: 23), wherein the performance of the DCO can be ascertained by a test circuit observing an output of the phase detector (In Yamaguchi, see fig. 29); and a variable phase accumulator coupled to the DCO and the phase detector, the variable phase accumulator containing circuitry to compute the variable phase. (In Girardeau, see fig. 1: 20)

Re claim 43, the combination of Girardeau and Yamaguchi further discloses a loop filter coupled to the phase detector and the DCO, the loop filter to provide a desired amount of attenuation to the computed difference between the reference phase and the variable phase. (In Girardeau, see fig. 1: 24)

Re claim 45, the combination of Girardeau and Yamaguchi further discloses that wherein the loop filter is comprised of a plurality of filters, and wherein the filters are arranged in a parallel fashion. (In Girardeau, see fig. 1: 24. One skilled in the art would know that the filters may be arranged either parallel or cascaded.)

Re claim 46, the combination of Girardeau and Yamaguchi further discloses that wherein the loop filter is comprised of a plurality of filters, and wherein the filters are arranged in a cascaded fashion. (In Girardeau, see fig. 1: 24. One skilled in the art would know that the filters may be arranged either parallel or cascaded.)

1. **Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Girardeau, Jr. (hereinafter Girardeau) (US patent 5,486,792) and Yamaguchi et al. (hereinafter Yamaguchi) (US Patent 6,687,629 B1), as applied to claim 1 above, and further in view of Kim et al (hereinafter Kim) (US Patent 6,885,700 B1).**

Re claim 2, the combination of Girardeau and Yamaguchi fails to specifically disclose that wherein the testing is performed using built-in self-test (BIST) techniques.

However, Kim does. (See abstract & col. 1, lines 13-40) Kim discloses a charge-based frequency technique that performs structural and defect-oriented testing and uses existing blocks to save die area.

Therefore, taking the combined teachings of Girardeau, Yamaguchi & Kim <u>as a whole</u>. It would have been obvious to one of ordinary skill in the art to have modified the system of Girardeau, as modified by Yamaguchi, in the manner as claimed and as taught by Kim, for the benefit of providing proper stimulus for the loop filter located inside the PLL.

Claims (10 & 44) are rejected under 35 U.S.C. 103(a) as being unpatentable over Girardeau, Jr. (hereinafter Girardeau) (US patent 5,486,792) and Yamaguchi et al. (hereinafter Yamaguchi) (US Patent 6,687,629 B1), as applied to claim 1 above, and further in view of Mathe et al (hereinafter Mathe) (US Patent 5,825,253).

Re claim 10, the combination of Girardeau and Yamaguchi fails to specifically disclose that wherein the all-digital phase-lock loop is operating in a type-I mode, and

the signal is an output of an infinite impulse response filter coupled to the output of a loop filter.

However, Mathe does. (See col. 5, lines 32-37) Mathe discloses a phase lock loop that contains a loop filter which can be implemented as a digital filter such as an infinite impulse response (IIR) filter.

Therefore, taking the combined teachings of Girardeau, Yamaguchi & Mathe as a whole. It would have been obvious to one of ordinary skill in the art to have modified the system Girardeau, as modified by Yamaguchi, in the manner as claimed, and as taught by Mathe, for the benefit of providing synthesis of both zeros and poles in the filter. (See col. 9, lines 55-56)

Re claim 44, the motivation for combining these two references has already been established in claim 10 above, therefore, the combination of Girardeau, Yamaguchi and Mathe further discloses that wherein the loop filter is of a type selected from a group consisting of a finite impulse response filter, an infinite impulse response filter or combination thereof. (In Mathe, see col. 5, lines 32-37 & col. 9, lines 55-56)

Claims (12 & 47) are rejected under 35 U.S.C. 103(a) as being unpatentable over Girardeau, Jr. (hereinafter Girardeau) (US patent 5,486,792) and Yamaguchi et al. (hereinafter Yamaguchi) (US Patent 6,687,629 B1), as applied to claim 1 above, and further in view of Koshiro et al (hereinafter Koshiro) (US Patent 5,768,326).

Re claim 12, the combination of Girardeau and Yamaguchi fails to specifically disclose that wherein the signal is an output of a gain normalization block.

However, Koshiro does. (See fig. 3: 31 & col. 11, lines 3-9) Koshiro discloses a PLL circuit where it is possible to normalized the output of the substractor, which is a diffrerence between PCR and the output of the counter. This normalization passes through the low-pass filter and is able to control the VCXO accurately.

Therefore, taking the combined teachings of Girardeau, Yamaguchi, and Koshiro as a whole. It would have been obvious to one of ordinary skill in the art to have modified the system Girardeau, as modified by Yamaguchi, in the manner as claimed, and as taught by Koshiro, for the benefit of controlling the VCXO accurately. (See col. 11, lines 3-9).

Re claim 47, the motivation for combining these two references has already been established in claim 10 above, therefore, the combination of Girardeau, Yamaguchi and Koshiro further disclose a gain normalization unit coupled to the phase detector and the DCO, the gain normalization unit to normalize the difference between the reference phase and the variable phase with respect to a gain in the DCO. (The references of Girardeau and Mathe disclose this limitation. Girardeau teaches a DPLL having a phase detector followed by a DCO. On the other hand, Koshiro teaches a normalization unit coupled in between a phase detector and a VCO. As a whole, these two references meet the limitations as claimed.)

Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Girardeau, Jr. (hereinafter Girardeau) (US patent 5,486,792) and Yamaguchi et al. (hereinafter Yamaguchi) (US Patent 6,687,629 B1), as applied to claim 1 above, and further in view of Gustafson et al (hereinafter Gustafson) (US Patent 4,086,539).

Re claim 18, the combination of Girardeau and Yamaguchi fails to specifically disclose that wherein if a variance in the magnitude is less than a specified threshold, then the frequency has been locked.

However, Gustafson does. (See abstract & col. 1, lines 37-40) Gustafson discloses that phase lock loops produce favorable results in terms of phase-error variance in high frequency system and below threshold.

Therefore, taking the combined teachings of Girardeau, Yamaguchi & Gustafson as a whole. It would have been obvious to one of ordinary skill in the art to have modified the system Girardeau, as modified by Yamaguchi, in the manner as claimed, and as taught by Gustafson, for the benefit of locking the frequency.

Claim 42 is rejected under 35 U.S.C. 103(a) as being unpatentable over Girardeau, Jr. (hereinafter Girardeau) (US patent 5,486,792) and Yamaguchi et al. (hereinafter Yamaguchi) (US Patent 6,687,629 B1), as applied to claim 41 above, and further in view of Knudsen (US Patent 7,079,611 B2).

Re claim 42, the combination of Girardeau and Yamaguchi fails to specifically disclose a time-to-digital converter (TDC) coupled to the DCO and the phase detector,

the TDC containing circuitry to compute a time difference between a reference clock and a variable clock.

However, Knudsen does. (See fig. 1 & col. 2, lines 14-25) Knudsen discloses a digital phase lock loop that computes the time difference of the clock input and the clock output.

Therefore, taking the combined teachings of Girardeau, Yamaguchi & Knudsen as a whole. It would have been obvious to one of ordinary skill in the art to have modified the system Girardeau in the manner as claimed, and as taught by Knudsen, for the benefit of providing useful information to a filter, which will be later on, to achieve synchronization. (See col. 2, lines 20-25)

7. Claims (1, 3-8, 11, 13-17, 19-22, 24, 27-31, 41, 43, 45-46) are rejected under 35 U.S.C. 103(a) as being unpatentable over Girardeau, Jr. (hereinafter Girardeau) (US Patent 5,486,792) in view of Wong et al. (hereinafter Wong) (US Patent 5,295,079)

Re claim 1, Girardeau discloses a method for testing a radio frequency (RF) circuit comprising: observing a signal from the RF circuit, wherein the signal is a digital signal from within a processing portion of the RF circuit (See fig. 2: 104), wherein the signal has a high degree of correlation with an RF output of the RF circuit (See fig. 1: the output of 23. Furthermore, it is well known in the art that both transmitters and receivers have PLLs) and manipulating the signal (See fig. 1: 23 & 24); and producing a

metric for the test based on results from the manipulating. (See fig. 1: 40 & 42 or 58 & 60)

But the reference of Girardeau fails to specifically disclose that wherein the observing occurs outside of the RF circuit.

However, Wong does. (See figs. 1 & 2: 4, col. 2, lines 38-40, col. 6-27) Wong discloses a digital tester configured to extract and interpret data from the PLL.

Therefore, taking the combined teachings of Girardeau and Wong as a whole. It would have been obvious to one of ordinary skills in the art to have incorporated this feature into the system of Girardeau, in the manner as claimed and as taught by Wong, for the benefit of optimizing the performance of the PLL.

Re claim 3, the combination of Girardeau and Wong further discloses that wherein the signal is a phase error signal. (In Girardeau, see fig. 1: 12, col. 2, lines 50-56)

Re claim 4, the combination of Girardeau and Wong further discloses that wherein the signal has a high degree of correlation with an RF output of the RF circuit. (One skilled in the art would know that if the input signal remains within a predetermined frequency, the PLL will produce an output signal having a frequency that is proportional to the clock input signal's frequency. Furthermore, when the PLL is in a lock mode, the output signal and the input signal are the same.)

Re claim 5, the combination of Girardeau and Wong further discloses that wherein a transfer function between the signal and the RF output phase is flat within a frequency band of interest. (One skilled in the art would know that if the output signal has a frequency that is proportional to the clock input signal's frequency, and if their similarities or relatedness are very high, then we can say that the output is some constant multiplied by the input. Furthermore, when the PLL is in a lock mode, the output signal and the input signal are the same.)

Re claim 6, the combination of Girardeau and Wong further discloses that wherein the RF circuit is an all-digital circuit, and wherein the signal is an output of a component in an all-digital phase-locked loop in the RF circuit. (In Girardeau, see fig. 1 & col. 2, lines 54-56)

Re claim 7, the combination of Girardeau and Wong further discloses that wherein the signal is an output of a phase detector. (In Girardeau, see fig. 1 & col. 2, lines 54-56)

Re claim 8, the combination of Girardeau and Wong further discloses that wherein the signal has been filtered. (In Girardeau, see fig. 1: 24 & col. 2, lines 62-65)

Re claim 9, the combination of Wong and Girardeau further discloses that wherein the all-digital phase-lock loop is operating in a type-11 mode, and the signal is

an output of an integral accumulator of a loop filter. (In Wong, see col. 3, lines 14-16, 50-52)

Re claim 11, the combination of Girardeau and Wong further discloses that wherein a loop filter coupled to an output of a phase detector performs the filtering, and wherein the signal is an output of the loop filter. (In Girardeau, see fig. 1: 24 & col. 2, lines 62-65)

Re claim 13, the combination of Girardeau and Wong further discloses that wherein the frequency of the signal is several orders of magnitude less than the frequency of the RF output. (It is inherent that the frequency of the error signal, outputted from the phase comparator, is less than the RF frequency.)

Re claim 14, the combination of Girardeau and Wong further discloses that wherein the test is for phase error trajectory and the signal is the output of a phase detector (In Girardeau, see fig. 1 & col. 2, lines 54-56), and wherein the manipulation comprises measuring a change in the signal. (In Girardeau, see fig. 2: error signal. And see col. 5, lines 37-39)

Re claim 15, the combination of Girardeau and Wong further discloses that wherein if the change in the signal is less than a specified threshold, then the phase error trajectory is good. (In Girardeau, see fig. 2: error signal. And see col. 5, lines 37-

39)

Re claim 16, the combination of Girardeau and Wong further discloses that wherein the measuring the change in the signal comprises measuring a peak, a variance, or a rate of change in the signal. (In Girardeau, see fig. 2: error signal. And see col. 5, lines 37-39)

Re claim 17, the combination of Girardeau and Wong further discloses that wherein the test is for frequency lock and the signal is the output of a phase detector (In Girardeau, see col. 2, lines 30-37 & col. 4, lines 65-67), and wherein the manipulation comprises comparing a value of the signal over several samples. (In Girardeau, see fig. 2 & col. 5, lines 37-40. The error signal is being compared with the threshold.)

Re claim 19, the combination of Girardeau and Wong further discloses that wherein the samples are taken at different times. (In Girardeau, see fig. 2 & col. 5, lines 37-40. The error signal is being compared with the threshold.)

Re claim 20, the combination of Girardeau and Wong further discloses that wherein the test is for frequency deviation and the signal is an output of an integral accumulator of a loop filter (In Girardeau, see col. 5, lines 19-21), and wherein the manipulation comprises comparing the signal with a specified range. (In Girardeau, see

col. 2, lines 30-36)

Re claim 21, the combination of Girardeau and Wong further discloses that wherein if the signal is within the specified range, then the frequency deviation is within acceptable limits. (In Girardeau, see col. 2, lines 30-36)

Re claim 22, the combination of Girardeau and Wong further discloses that wherein the manipulation further comprises comparing several samples of the signal. (In Girardeau, see fig. 2 & col. 5, lines 37-40. The error signal is being compared with the threshold.)

Re claim 23, the combination of Wong and Girardeau further discloses that wherein the RF circuit contains an all-digital phase-locked loop operating in a type-II mode. (In Wong, see col. 3, lines 14-16, 50-52)

Re claim 24, the combination of Girardeau and Wong further discloses that wherein the RF circuit contains an all-digital phase-locked loop, and the method further comprises prior to the observing, setting the all-digital phase-locked loop to a certain bandwidth. (In Girardeau, see col. 5, lines 19-21. Furthermore, it is inherent that the loop bandwidth, also referred as the unity loop gain frequency, of the phase lock loop is set prior to start up.)

Re claim 27, the combination of Girardeau and Wong further discloses that wherein the RF circuit is an all-digital frequency synthesizer. (In Girardeau, see col. 5, line 20)

Re claim 28, the combination of Girardeau and Wong further discloses that wherein the RF circuit is an all-digital transmitter. (In Girardeau, see col. 1, lines 24-27)

Re claim 29, the combination of Girardeau and Wong further discloses that wherein the transmitter is used in a wireless communications network. (In Girardeau, see col. 1, lines 24-27)

Re claim 30, the combination of Girardeau and Wong further discloses that wherein the wireless communications network is Bluetooth compliant. (In Girardeau, see col. 1, lines 24-27. It is inherent that the network is Bluetooth compliant.)

Re claim 31, the combination of Girardeau and Wong further discloses that wherein the testing comprises a functional test or a compliance test of the RF circuit. (In Girardeau, see col. 2, lines 30-37 & col. 5, lines 10-21)

Re claim 35, the combination of Wong and Girardeau further discloses that wherein the first and the second integrated circuits are the same integrated circuit. (In

Girardeau, see fig. 1)

Re claim 36, the combination of Wong and Girardeau further discloses that wherein the RF circuit contains an all-digital phase-locked loop, and wherein the processor is coupled to an output of a phase detector. (In Girardeau, see fig. 1: element 18. The adjuster can be considered to be a processor.)

Re claim 41, the motivation for combining these two references has already been established in claim 1 above, therefore, the combination of Girardeau and Wong further discloses a circuit comprising: a reference phase accumulator coupled to a signal input, the reference phase accumulator containing circuitry to compute a reference phase (In Girardeau, see fig. 1: 26); a phase detector coupled to the reference phase accumulator, the phase detector containing circuitry to compute a difference between the reference phase and a variable phase (In Girardeau, see fig. 1: 12); a digitally-controlled oscillator (DCO) coupled to the phase detector (In Girardeau, see fig. 1: 23), wherein the performance of the DCO can be ascertained by a test circuit observing an output of the phase detector (In Wong, see fig 2: 26, col. 3, lines 50-55); and a variable phase accumulator coupled to the DCO and the phase detector, the variable phase accumulator containing circuitry to compute the variable phase. (In Girardeau, see fig. 1: 20)

Re claim 43, the combination of Girardeau and Wong further discloses a loop filter coupled to the phase detector and the DCO, the loop filter to provide a desired amount of attenuation to the computed difference between the reference phase and the variable phase. (In Girardeau, see fig. 1: 24)

Re claim 45, the combination of Girardeau and Wong further discloses that wherein the loop filter is comprised of a plurality of filters, and wherein the filters are arranged in a parallel fashion. (In Girardeau, see fig. 1: 24. One skilled in the art would know that the filters may be arranged either parallel or cascaded.)

Re claim 46, the combination of Girardeau and Wong further discloses that wherein the loop filter is comprised of a plurality of filters, and wherein the filters are arranged in a cascaded fashion. (In Girardeau, see fig. 1: 24. One skilled in the art would know that the filters may be arranged either parallel or cascaded.)

8. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Girardeau, Jr. (hereinafter Girardeau) (US patent 5,486,792) and Wong et al. (hereinafter Wong) (US Patent 5,295,079), as applied to claim 1 above, and further in view of Kim et al (hereinafter Kim) (US Patent 6,885,700 B1).

Re claim 2, the combination of Girardeau and Wong fails to specifically disclose that wherein the testing is performed using built-in self-test (BIST) techniques.

However, Kim does. (See abstract & col. 1, lines 13-40) Kim discloses a charge-based frequency technique that performs structural and defect-oriented testing and uses existing blocks to save die area.

Therefore, taking the combined teachings of Girardeau, Wong & Kim as a whole. It would have been obvious to one of ordinary skill in the art to have modified the system of Girardeau, as modified by Wong, in the manner as claimed and as taught by Kim, for the benefit of providing proper stimulus for the loop filter located inside the PLL.

Claims (10 & 44) are rejected under 35 U.S.C. 103(a) as being unpatentable over Girardeau, Jr. (hereinafter Girardeau) (US patent 5,486,792) and Wong et al. (hereinafter Wong) (US Patent 5,295,079), as applied to claim 1 above, and further in view of Mathe et al (hereinafter Mathe) (US Patent 5,825,253).

Re claim 10, the combination of Girardeau and Wong fails to specifically disclose that wherein the all-digital phase-lock loop is operating in a type-I mode, and the signal is an output of an infinite impulse response filter coupled to the output of a loop filter.

However, Mathe does. (See col. 5, lines 32-37) Mathe discloses a phase lock loop that contains a loop filter which can be implemented as a digital filter such as an infinite impulse response (IIR) filter.

Therefore, taking the combined teachings of Girardeau, Wong & Mathe as a whole. It would have been obvious to one of ordinary skill in the art to have modified the system Girardeau, as modified by Wong, in the manner as claimed, and as taught

by Mathe, for the benefit of providing synthesis of both zeros and poles in the filter. (See col. 9, lines 55-56)

Re claim 44, the motivation for combining these two references has already been established in claim 10 above, therefore, the combination of Girardeau, Wong and Mathe further discloses that wherein the loop filter is of a type selected from a group consisting of a finite impulse response filter, an infinite impulse response filter or combination thereof. (In Mathe, see col. 5, lines 32-37 & col. 9, lines 55-56)

Claims (12 & 47) are rejected under 35 U.S.C. 103(a) as being unpatentable over Girardeau, Jr. (hereinafter Girardeau) (US patent 5,486,792) and Wong et al. (hereinafter Wong) (US Patent 5,295,079), as applied to claim 1 above, and further in view of Koshiro et al (hereinafter Koshiro) (US Patent 5,768,326).

Re claim 12, the combination of Girardeau and Wong fails to specifically disclose that wherein the signal is an output of a gain normalization block.

However, Koshiro does. (See fig. 3: 31 & col. 11, lines 3-9) Koshiro discloses a PLL circuit where it is possible to normalized the output of the substractor, which is a diffrerence between PCR and the output of the counter. This normalization passes through the low-pass filter and is able to control the VCXO accurately.

Therefore, taking the combined teachings of Girardeau, Wong, and Koshiro as a whole. It would have been obvious to one of ordinary skill in the art to have modified

the system Girardeau, as modified by Wong, in the manner as claimed, and as taught by Koshiro, for the benefit of controlling the VCXO accurately. (See col. 11, lines 3-9).

Re claim 47, the motivation for combining these two references has already been established in claim 10 above, therefore, the combination of Girardeau, Wong and Koshiro further disclose a gain normalization unit coupled to the phase detector and the DCO, the gain normalization unit to normalize the difference between the reference phase and the variable phase with respect to a gain in the DCO. (The references of Girardeau, Wong and Mathe disclose this limitation. Girardeau teaches a DPLL having a phase detector followed by a DCO. On the other hand, Koshiro teaches a normalization unit coupled in between a phase detector and a VCO. As a whole, these two references meet the limitations as claimed.)

Claims (18, 25, 26) are rejected under 35 U.S.C. 103(a) as being unpatentable over Girardeau, Jr. (hereinafter Girardeau) (US patent 5,486,792) and Wong et al. (hereinafter Wong) (US Patent 5,295,079), as applied to claim 1 above, and further in view of Gustafson et al (hereinafter Gustafson) (US Patent 4,086,539).

Re claim 18, the combination of Girardeau and Wong fails to specifically disclose that wherein if a variance in the magnitude is less than a specified threshold, then the frequency has been locked.

However, Gustafson does. (See abstract & col. 1, lines 37-40) Gustafson discloses that phase lock loops produce favorable results in terms of phase-error variance in high frequency system and below threshold.

Therefore, taking the combined teachings of Girardeau, Wong & Gustafson as a whole. It would have been obvious to one of ordinary skill in the art to have modified the system Girardeau, as modified by Wong, in the manner as claimed, and as taught by Gustafson, for the benefit of locking the frequency.

Re claim 25, the combination of Girardeau, Wong and Gustafson further discloses that wherein the test is for estimating phase noise power (In Girardeau, see col. 5, lines 19-21. The DPLL is able to operate in noisy condition. At some point in the process, the noise has to be determine in order to accurately lock the frequency.), and the signal is an output of a phase detector (In Girardeau, see fig. 1: the output of element 12), wherein the manipulating comprises calculating a mean square error of the signal. (In Gustafson, see col. 2, lines 1-3)

Re claim 26 the combination of Girardeau, Wong and Gustafson further disclose that wherein the setting, observing, and manipulating is repeated for several different all-digital phase-locked loop bandwidths, and wherein the producing comprises subtracting the calculated mean square errors for the several different all-digital phase-lock loop bandwidths. (One skilled in the art would know that when a PLL is under testing, each of its parameters must be tested in order to obtain optimum performance.)

Claim 42 is rejected under 35 U.S.C. 103(a) as being unpatentable over Girardeau, Jr. (hereinafter Girardeau) (US patent 5,486,792) and Wong et al. (hereinafter Wong) (US Patent 5,295,079), as applied to claim 1 above, and further in view of Knudsen (US Patent 7,079,611 B2).

Re claim 42, the combination of Girardeau and Wong fails to specifically disclose a time-to-digital converter (TDC) coupled to the DCO and the phase detector, the TDC containing circuitry to compute a time difference between a reference clock and a variable clock.

However, Knudsen does. (See fig. 1 & col. 2, lines 14-25) Knudsen discloses a digital phase lock loop that computes the time difference of the clock input and the clock output.

Therefore, taking the combined teachings of Girardeau, Wong & Knudsen <u>as a whole</u>. It would have been obvious to one of ordinary skill in the art to have modified the system Girardeau in the manner as claimed, and as taught by Knudsen, for the benefit of providing useful information to a filter, which will be later on, to achieve synchronization. (See col. 2, lines 20-25)

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leon Flores whose telephone number is 571-270-1201. The examiner can normally be reached on Mon-Fri 7-5pm Alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Payne can be reached on 571-272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

LF
September 7, 2007

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